## ABSTRACT OF THE DISCLOSURE

**[45]** Systems and methods are disclosed for reducing or eliminating hot carrier injection stress in circuits. In one embodiment, the present invention relates to an integrated circuit comprising an IO PAD, an output circuit coupled to at least the IO PAD and a stress circuit. The stress circuit is coupled to at least the output circuit and is adapted to limit a high voltage across the output circuit when the output circuit is enabled, thereby reducing stress on the output circuit. In one embodiment, the stress circuit comprises at least one transistor device (a p-channel device or two stacked p-channel devices, for example) and the output circuit comprises a transistor device (an n-channel device or two stacked n-channel devices).